D2a

Partial Translation of D2 (JP H07-045948 A)

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Title: Multilayer Wiring Board and Process for Making Same

Claim 1

A multilayer circuit board (6,7) comprising interlaminar insulating layers made of a resin (I_1, I_2, I_3, I_4) and metal conductor patterns (C_2, C_3, C_4, C_5, C_6), which interlaminar insulating layers and the metal conductor patterns are alternately laminated on a substrate board (1,4), wherein the metal conductor patterns (C_2 - C_6) comprises a metal thin film layer (L_1) formed by sputtering a metal capable of enhancing adhesion of the metal conductor patterns (C_2 - C_6), and a copper plated layer (L_3) formed on the metal thin film layer (L_1).

Claim 2

A multilayer circuit board (6,7) comprising interlaminar insulating layers made of a resin (I_1, I_2, I_3, I_4) and metal conductor patterns (C_2, C_3, C_4, C_5, C_6), which interlaminar insulating layers and the metal conductor patterns are alternately laminated on a substrate board (1,4), wherein the metal conductor patterns (C_2 - C_6) comprises a metal thin film layer (L_1) formed by sputtering a metal capable of enhancing adhesion of the metal conductor patterns (C_2 - C_6), a copper thin film layer (L_2) formed by sputtering copper on the metal thin film layer (L_1), and a copper plated layer (L_3) formed on the copper thin film layer (L_2).

Page 4, paragraphs [0021], [0023]

A first conductor pattern composed of one or, if desired, more kinds of metal is formed on the above-mentioned substrate board by a conventional film forming procedure such as, for example, sputtering. ..(partially omitted)..

As specific examples of the resin constituting the

interlaminar insulating layers, there can be mentioned, for example, polyimdie resin, polyamide resin, epoxy resin, BT(bismaleimide-triazine) resin, BCB (divinylsiloxanebisbenzocyclobutene) resin, polyester resin, modified polyimide resin, modified BT resin, modified epoxy resin, triazine resin, polybutadiene resin, polysulfone resin, polyether-polysulfone resin, polyetherimide resin, polyphenylene oxide resin, phenolic resin and urea resin.

Page 5, paragraphs [0028], [0029]

On the surface-treated first interlaminar insulating layer, a metal thin film layer composed of a metal capable of enhancing adhesion of a metal conductor pattern is formed. Further, on the metal thin film layer, a copper thin film layer is formed by sputtering copper. Thus, a primary layer composed of one or two kinds of metals is formed on the surface-treated first interlaminar insulating layer.

The metal capable of enhancing adhesion of a metal conductor pattern includes, for example, chromium, nickel, titanium, iron, tungsten, molybdenum, aluminum and cobalt. The metal thin film layer formed by sputtering such metal is densified and has smooth surface, and exhibits high adhesion to the interlaminar insulating layer.

PATENT ABSTRACTS OF JAPAN

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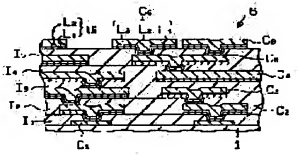
(54) MULTILAYER WIRING BOARD AND ITS MANUFACTURE

(57)Abstract:
PURPOSE: To obtain a conductor pattern hard to strip even when an interlayer insulating layer is not roughened by chemicals by a method wherein the conductor pattern is constituted of a metal thin layer formed in such a way that a metal capable of enhancing the close contact property of the conductor pattern has been sputtered and of a copper-plated layer formed on the metal thin layer.
CONSTITUTION: Since a multilayer wiring board 6 uses a metal such as chromium or the like capable of enhancing the close contact property of conductor latterns C1 to C5 as a metal for formation of a metal thin film, it is possible to obtain the conductor patterns hard to strip. In addition, a metal thin layer L1 formed by a sputtering operation is generally dense and smooth, and its adhesion force is excellent. As a result, the metal thin layer TL is used as a substratum for a copper-plated layer L3, and the close contact property of the conductor patterns C1 to C5 can be enhanced even when interlayer insulating layers I1 to I5 are not roughened by chemicals.



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CLAIMS

[Claim(s)]
[Claim 1] In the multilayer-interconnection plate (6 7) which comes to carry out laminating formation of the layer insulation layer made of resin (I1, I2, I3, I4, and I5), and the metal conductor pattern (C2, C3, C4, C5, and C6) on a substrate (1 4) by turns The metal thin layer formed by carrying out sputtering of the metal which may improve the adhesion of a conductor pattern (C2 - C6) (L1), The multilayer-interconnection plate equipped with the conductor pattern (C2 - C6) constituted by the copper-plating layer (L3) formed on said metal thin layer (L1).
[Claim 2] In the multilayer-interconnection plate (6 7) which comes to carry out laminating formation of the layer insulation layer made of resin (I1, I2, I3, I4, and I5), and the metal conductor pattern (C2, C3, C4, C5, and C6) on a substrate (1 4) by turns The metal thin layer formed by carrying out sputtering of the metal which may improve the adhesion of a conductor pattern (C2 - C6) (L1), The multilayer-interconnection plate equipped with the conductor pattern (C2 - C6) constituted by the copper thin layer (L2) formed by carrying out sputtering of the copper on said metal thin layer (L1), and the copper-plating layer (L3) formed on said copper thin layer (L2).
[Claim 3] In the manufacture approach of the multilayer-interconnection plate (6 7) which carries out laminating formation of the layer insulation layer made of resin (I1, I2, I3, I4, and I5), and the metal conductor pattern (C2, C3, C4, C5, and C6) by turns on a substrate (1 4) It is following (a) at least. - (a) The manufacture approach of the multilayer-interconnection plate characterized by performing a process one by one : (a) By carrying out the spin coat of the resin on a substrate (1 4) The process and (b) which form a layer insulation layer (I1 -I5) By performing reverse sputtering to said layer insulation layer (I1 -I5) The process and (c) which process the front face of said layer insulation layer (I1 -I5) By carrying out sputtering of the metal which may improve the adhesion of a conductor pattern (C2 - C6), and carrying out sputtering of the copper if needed The process which forms the substrate layer (UL) which consists of one sort or two sorts of metals on the processing side (TS) of said layer insulation layer (I1 -I5),

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to a multilayer-interconnection plate and its manufacture approach.
[0002]
[Description of the Prior Art] When realizing a large-scale and high-speed computer system etc., small IC chip of high accumulation etc. is usually used, and it becomes an important technical problem to make it into the structure suitable for improvement in the speed, and to mount in a patchboard. For this reason, in recent years, improvement in the speed and the cures against dansification, such as multilayering, and thinning, thin-film-izing of a conductor pattern (the so-called finization), are demanded also about the patchboard for carrying IC chip etc.
[0003] As an approach of forming a metal conductor pattern in a patchboard, the subtractive process which uses copper clad laminate as a start ingredient is widely known from before. Moreover, recently, the additive process which forms a conductor pattern only with nonelectrolytic pleting attracts attention as an option which changes to a subtractive process. Here, the manufacture procedure of the common multilayer-interconnection plate by the additive process (fully-additive process) is described briefly.
[0004] First, the adhesives for additives for forming a layer insulation layer are applied to the substrate front face which has a inner layer conductor pattern by the roll coater etc. These adhesives make a resin matrix distribute a meltable filler to a roughening agent. After said adhesives pass through exposure development and hardening processing, they are roughened by roughening agents, such as a chromic acid. Consequently, the filler in an adhesives layer is dissolved partially and a roughening side is formed in the front face of an adhesives layer. A catalyst nucleus required for the deposit of the beginning of pleting is given to the roughening side of an adhesives layer, and plating resist is further formed of exposure development. Then, a conductor pattern is formed by performing non-electrolytic copper plating to a resist agenesis part.
[0005] By repeating the procedure of the above conductor pattern formation if needed, the so-called build up multilayer-interconnection plate with which laminating formation of a layer insulation layer and the conductor pattern was carried out by turns on the substrate can be obtained.
[0006]
[Problem(s) to be Solved by the Invention] However, in the conventional full additive process, since the adhesives spreading, roughening, catalyst nucleus grant, and redio solution copper plating process of having mentioned above are required, the whole activity is complicated. However, the predetermined adhesion force is secured between layer insulation layers, and in order to obtain the conductor pattern which cannot exfoliate easily, there is a situation that neither of the above-mentioned processes can be skipped.
[0007] Moreover, in the full additive process, the roll coater is used as a general means to apply adhesives to a substrate front face. A roll coater has an parallel slot and is conventionally known as a coater which consists of a doctor bar arranged by approaching the roll of the pair arranged by separating a predetermined gap, and an upper roll.
[0008] However, even if it is going to apply adhesives thinly using such equipment, thickness control becomes difficult and the problem that a smooth and uniform layer insulation layer cannot be obtained arises. In this case, by roughening of a layer insulation layer, irregularity becomes easy to be made on a front face, and the formation precision of a conductor pattern, the electrical property of a patchboard, etc. will get worse as a result.
[0009] Furthermore, the chemicals used at a roughening process have many harmful things to the body like a chromic acid or potassium permanganate generally. Therefore, the manufacturer of a patchboard needs to plan a certain antipollution measure like discarding chemicals carefully etc. However, when such a cure is performed, there is a problem of becoming cost quantity inevitably.
[0010] This invention is made in view of the above-mentioned situation, and the 1st purpose is in offering the multilayer-interconnection plate which can obtain the conductor pattern which cannot exfoliate easily, without roughening the layer insulation layer by chemicals.
[0011] The 2nd purpose of this invention is to offer the manufacture approach of the multilayer-interconnection plate which can raise the smooth nature of a layer insulation layer, and homogeneity since the thickness control of a layer insulation layer is easy, and can raise adhesion, formation precision, etc. of a conductor pattern certainly.
[0012] The 3rd purpose of this invention can simplify a production process, and is to offer the manufacture approach of the multilayer-interconnection plate which can moreover reduce a manufacturing cost.
[0013]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, in invention according to claim 1 In the multilayer-interconnection plate which comes to carry out laminating formation of the layer insulation layer made of resin, and the metal conductor pattern on a substrate by turns The multilayer-interconnection plate equipped with the conductor pattern constituted by the metal thin layer formed by carrying out sputtering of the metal which may improve the adhesion of a conductor pattern, and the copper-plating layer formed on said metal thin layer is made into the summery.
[0014] In the multilayer-interconnection plate which comes to carry out laminating formation of the layer insulation layer made of resin, and the metal conductor pattern on a substrate in invention according to claim 2 by turns The metal thin layer formed by carrying out sputtering of the metal which may improve the adhesion of a conductor pattern, The multilayer-interconnection plate equipped with the conductor pattern constituted by the copper thin layer formed by carrying out sputtering of the copper on said metal thin layer and the copper-plating layer formed on said copper thin layer is made into the summary.
[0015] In the manufacture approach of the multilayer-interconnection plate which carries out laminating formation of the layer insulation layer made of resin, and the metal conductor pattern by turns on a substrate in invention according to claim 3 It is following (a) at least. - (a) Process, i.e., (a), By carrying out the spin coat of the resin on a substrate The process end (b) which form a layer insulation layer By performing reverse sputtering to said layer insulation layer The process end (c) which process the front face of said layer insulation layer By carrying out sputtering of the metal which may improve the adhesion of a conductor pattern, and carrying out sputtering of the copper if needed The process and (d) which form the substrate layer which consists of one sort or two sorts of metals on the processing side of said layer insulation layer By giving copper plating, where plating resist is formed on said substrate layer The process end (e) which form a copper-plating layer in the predetermined part on said substrate layer By etching the substrate layer located said plating resist and under the plating resist The manufacture approach of the multilayer-interconnection plate characterized by performing the process which forms the conductor pattern constituted by a substrate layer and the copper-plating layer one by one is made into the summary.
[0016] In the manufacture approach of the multilayer-interconnection plate which carries out laminating formation of the layer insulation layer made of resin, and the metal conductor pattern by turns on a substrate in invention according to claim 4 It is following (a) at least. - (f) Process,

i.e., (a), By carrying out tha spin coet of the resin on a substreta The process end (b) which form e layer insulation leyar By performing reverse sputtering to seid leyer insulation leyar The process and (c) which process the front face of seid leyer insulation leyer By carrying out sputtering of the metal which may improve the adhesion of e conductor pettern, and carrying out sputtering of the coppar if needed The process and (d) which form the substrete layer which consists of one sort or two sorts of metals on tha processing sida of seid layer insuletion leyar By etching, where e resist is formed on said substrate leyer The process and (a) which make tha substrete layer the shepe of e predetermined pettern The process end (f) which exfoliete seid rasist from the substrate layer etched in the shepe of a pettern By performing non-alectrolytic coppar pleting or electrolytic copper plating to seid substrete layer The manufacture approech of the multilayar-interconnection plata cheractarizad by performing tha process which forms the conductor pattern constituted by a substrata layer end the copper-plating layer ona by one is made into tha summary.

[0017]

[Function] Since the matal which may improve tha adhesion of e conductor pattern ea e metel for metal thin film formetion is used according to tha multilayer-interconnection plete of this invention, tha conductor pattern which cennot exfoliate aesily cen be obtained. Moreover, in this invention, being formad by the physicel forming-membranes mathod of sputtering characterizas e metal thin layer. And generally the metal thin layer by sputtaring is precise and smooth, end becoming the thing excellent in adhesion force is known. Therefore, even if it does not roughan tha layer insulation layer by chamicels according to this invention from which such a metal thin layer sarves as a substrate of a copper-plating leyer, it becomas possible to reise the edhesion of e conductor pattern.

[0018] And since [according to tha menufecture approach of the multileyer-interconnection plate of this invention] rasin is applied with e spin coet, evan when it is going to obtain tha layer insuletion layer of closing in, thickness control can be performed aasily. Therafore, the smooth netura of a layer insuletion leyar end homogeneity can be raised, end edhesion, formetion precision, atc. of a conductor pettarn cen be certainly reisad as the result. Since the front face of a layer insuletion leyer will ba procassed by raverse sputtering, it becomas unnecessary moreovar, to parform roughening by chamicals in advenca of formetion of a conductor pettern according to this menufactura approach. Tharafore, a production process is simplified and, moreover, e manufacturing cost is reduced.

[0019] Heraaftar, tha menufactura approach is explained to e datail for the multileyer-intarconnection plata of this invention in order of e process. In this invention, the substrata made of tha product made from a ceramic sintered compact, metal, and a plastic can ba usad as e substrate for carrying out leminating formetion of a layer insuletion layer and the conductor pettern by turns.

[0020] As e substrata made from e ceremic sintered compact, there are an alumimium nitride (AlN) substrete, an elumine (aluminum 2O3) aubetrate, a boron nitride (BN) substrata, a silicon nitride (Si3N4) substrate, a mullite (3aluminum2 O3 and 2SiO2) substrata, etc., for example. As a metal eubstrete, there ere a phosphor bronze aubstrate, an aluminum (aluminum) subatrata, an alumite substrete, en iron (Fe) substrete, e copper (Cu) substrata, atc., for axampla. When producing the multileyer-interconnection plete which thought haat dissipation natura etc. as important, it is good to choose the substrate made from e ceremic sintered compact, end it good to choose an elumimium nitride substrete especially with high thermal conductivity especiely. Moreover, when producing the multileyer-interconnection plate which thought low cost neture, workebility, etc. es important, it is desirable to choose the substrate made of metal or a plastic.

[0021] The conductor pettern of the 1st leyer which consists of ona sort or two or more sorts of metals by the conventionelly well-known forming-membranas method of sputtering atc. if naedad is formed in the front face of said substrate. In order to form a leyar [1st] layer insulation leyer on the substrate with which the conductor pettern wes formad, tha spin coet of the resin of photosensaitiva or nonphotosensitivity is cerried out. A spin coet method is the method of eppliceticn which is made to rotate e substrate where e fluid is supplied on the substrate laid horizontally, and spreads a fluid over homogeneity thinly according to a centrifugal force at the whole substrata. And in enforcing such a spin coet method, the coeter called a spin coater is usuelly usad.

[0022] As resin for leyer insuletion leyers, thare ere polyimide resin, polyamide resin, en epoxy resin, BT (bismaleimida triazine) resin, BCB (divinyl siloxene screw benz-cyclo-butene) resin, polyaster resin, convarsion polyimide resin, convarsion BT resin, e conversion epoxy resin, triazine resin, e polybutadiene resin, Pori Sall John resin, polyether ape phon resin, polyetherimida resin, polyphanylane oxide resin, phanol rasin, a urae rasin, atc., for exemple.

[0023] It is dasirable to choose a comparativaly cheap thing like en epoxy resin or BT resin aspecially as resin to be used. The reason is advantageous [using these rasin / like], when attaining low cost-ization of e multilayar-interconnaction plata. Moreover, it is desirable to choose what hes the emount of hardening contraction amall in choosing what has low reactivity with copper es rasin to ba used. As rasin which fulfills tha abova-mantionad conditions, thera are en epoxy resin, BT resin, atc., for axempla.

[0024] In eddition, it is desirable to give photosansitivity to the resin for layer insulation stratificetion anumarsted previously. The reason is photolithographies, such as exposura and development, can ba performed end possible [reising the formation precision of a layer insulation layer more], if it is resin which gave photosensitivity. Moreover, the hole for forming the interstatiel vie hole (it only abbrevieting to IVH hereefter) which eims at the electric flow betwean each class is formed in a layer insuletion layer if needed.

[0025] As for the thickness of the rasin applied by tha spin coatar, it is good thet it is 5 micrometers - about 70 micrometers, end, as for the thicknass of tha layar insulation leyer finelly obtained, it is good that it is 3 micrometars - about 50 micrometers. The case where it becomes impossible to cover e conductor pattarn with resin completely as the thicknass of the resin epplied is less then 5 micrometers mey eriae. When this thicknesa exceade 50 micrometers, it becomes impoesible on the other hand, to amploy the adventaga of a spin coat mathod efficiantly. Moraover, it is because it is dasirable whan attaining lamination of tha whole petchboerd, holding e suitable alectricel property to make thicknass of a layer insuletion layar into eeid within the limits.

[0026] Next, tha procadura which forme tha conductor pattarn and layer ineulation layer aftar the 2nd layer is explained. In advance of matalad sputtering, reverse sputtering is performed in a layar [1st] layar insuletion layer. Raversa sputtering points out the thing of sputtering parformed by making a target matarial side in cathoda the bottom of en inert gee embiant atmosphere, and making reverse tha aforamantionad cathode end enode plete unlike tha ueual sputtering which makas a substrate side en anode plata end performs it. That is, whan revarae sputtering is carried out, tha ion of inert gas cen draw naer to a substrata side, and the front face of a substrata will ba procaased by the impect et that time. And so to speak, "it will be roughenad physicelly" by the front face of e layer inaulation layer by passing through auch reverse sputtering. The adventage of processing by such reversa sputtering is baing eble to perform mataled sputtering immedietely within tha equipmant sama efter processing.

[0027] As inert gas filled in a high vecuum tub at tha time of reversa aputtering, thera ere nitrogen, an argon, helium, neon, e krypton, atc., for example. Whan inert gas is used as an ergon, thare is an edventege thet the adhesion of the metal thin layar formad of aputtering becomee good. Moreover, when inert gas is used as nitrogen, the rasidua whan atching a metal thin layer stops baing eble to remein easily, and thare is an advantage that tha insuletion between conductor patterns becomes good.

[0028] On tha processing side of the layar [1st] layar inaulation layer by which aurface treatmant was cerried out, e metal thin layar is formed of metalad aputtering which mey improve the adhasion of e conductor pattern. And on this metal thin layar, a coppar thin leyar is formed of coppar sputtering. Consequantly, it will ba in the condition that the substrete layer which consists of one sort or two sorts of matals was praperad on the processing side of a leyer insuletion leyer.

[0029] The metal which mey improva the edhasion of a conductor pettarn hare points out chromium, nickel, titanium, iron, e tungsten, molybdenum, eluminum, cobelt, etc. The metal thin layar obtained by sputtering of these metals is precise and smooth, end it is because it becomes

the thing excellent in the adhesion force to a layer insulstion lsyer. Morsover, it is becsuse the sbove-mentionsd metal thin lsyer is easily removabls with the etchsnt of the simple presentation which does not contain an oxidizing agent, so it is convenient to pattern formstion. In the sdhssion of coppsr pleting to s mstal thin lsyer, said coppsr thin lsysr is formed if needed, in ordsr to raise the edhesion betwssn haight, e copper-plsting lsyer, snd s mstal thin lsyer.
[0030] In this cass, it is desirebls to sst thickness of a metal thin lsyer to 0.05 micromsters - sbout 0.3 micrometers. snd to set thickness of s copper thin lsyer to 0.05 micromsters - about 0.6 micromstsrs. Moreover, as for the thickness in the total of s substrste layer, it is good thet it is sbout 1.0 micrometers or less.
[0031] Dispersion srises that the thickness of a metsl thin film is below ssid range in adhesion with a lsyer insulstion leyer, end it becomes eesy to produce un-arranging, such ss exfoliation end bulging. On the other hend, slthough time emount and cost start sputtering as the thickness of e mstal thin lsyer is ebove said range, there is no great differsncs in the effectiveness acquired. There is e possibility thet it may become impossible to fully improve the edhesion of a coppsr-pleting lsyer ss the thickness of e copper thin lsyer is below said renge. On the other hsnd, slthough time smount snd cost start sputtering es the thickness of a copper thin lsyer is ebovs ssid renge, there is no greet difference in the effectivenese acquired.
[0032] In eddition, when nickel is chosen ss e metal which carries out sputtering, it is slso possibls to omit sputtering of the coppsr to s metal thin leyer top. The reeson of the edhesion of copper plating to nickel is comperetively good, snd is becsuse it msy be necessary to necesssrily form s copper thin leyer.
[0033] Predetermined plsting resist is formed on e substrate lsyer, snd electrolytic copper plsting or non-elsctrolytic copper pleting is performed in this condition. Consequently, s copper-plsting layer is formed in the front fsce of a substrste lsyer.
[0034] Since it is the metsl lsyer which functions as a substsntiel conductor lsyer for meking it flow through the elsctricsl end elsctric equipment, said copper-plsting lsyer is formed a little more thickly compsrsd with s substrste lsyer. However, when s copper-pleting lsysr bscomes thick too much, e surface levsl difference becomes lsrge and a possibility of csusing trouble is in spresding of the resin by the spin coeter. Whsn an example is taken in this situstion, it is good to set up the thickness of s copper-plsting lsyer within the limits of 2 micrometers - 10 micrometers more preferably within ths limits of 2 micrometers - 30 micrometers.
[0035] After forming a copper-pleting lsyer, the substrate leyer located plating resist which beceme unnecessary, and under the plsting resist is removed by etching. The conductor psttern of the 1st lsyer constituted by ths substrste leyer which consists of one sort or two sorts of metals by this processing, and the coppsr-plsting lsyer is obteined.
[0036] In this csse, in order to sttsin shortening snd process simplificstion of production time, it is dssirsble like copper, nickel and copper, chromium end copper, and titanium to use the etchant which csn dissolve two or more sorts of metals in coincidence. As sn exemple of the above etchsnt, the mixed wster solution of the fluoric acid snd the nitric ecid which mey dissolve coppsr end nickel in coincidence is mentioned.
[0037] Moreover, where s resist is formsd beforehsnd, after etching e substrsts lsyer in the shepe of s psttsrn es sn spproech of forming the conductor psttern of the 1st layer, it is elso possible to taks ths spproach of exfoliating the resist and forming a copper-pleting layer. And on the substrate in which the conductor pattern was formed by one of approaches, s lsyer [2nd] lsysr insulstion leyer is formsd by csrrying out the spin coat of the resin agsin. And the above processses (formetion of the substrete layer by the spin coet of resin and sputtering snd formstion of a copper-plsting leyer) are psrformed repeatedly if needed.
[0038]
[Working Exsmple(s) and Compsretive Exsmple(s)] Hersafter, ths examples 1-11 which materielized this invention, end ths sxemple of s compsrison of those are expleined to a detail based on e drawing.
[Exemple 1]
process (1): — as s substrste — ths phosphor bronze substrete (Cu:Sn-=95:4.8:0.2) 1 — choosing — conductor psttern C1 of the 1st lsyer on this phosphor bronze substrste 1 mslsnism — it processed.
[0039] Process (2): The photosensitive spoxy resin which consists of the following presentation es resin for lsyer insulation stratificstion was prepersd.
Crssol novolak scrylate resin: 66 % of the weight, bisphenol A mold resin:21 % of the wsight Sensitizsr: 6 % of the weight, curing sgent:3 % of the weight Photopolymerizetion agent: 3 % of the weight Intsrfecs regulstor: As shown in 1 % of the weight . end drawing 1 (s), this resin wss epplied on the phosphor bronze substrate 1 using the spin coster (the Miksss, Inc mske, trsde nsme:lH-DX). In eddition, layer insulation layer 11 finally obtained In this example, the thicknsss of the resin to apply was set as 30 micrometers so thet thickness might be set to 20 micrometers.
[0040] Process (3): After prebeking s photosensitive epoxy resin, exposure and development were performed end 180 dsgrees C and cure processing for 60 minutes were further performed to the photosensitive epoxy resin. Layer [1st] lsyer insulstion leyer 11 equipped with the hole 2 with a diameter of about 30 micrometers for IVH formetion by the above processing as shown in drswing 1 (b) It obtained.
[0041] Process (4): Next use a vacuum sputtering system (meds in the Tokude fsctory, CFS-8EP), snd it is the lsyer insulation layer 11 in nitrogen-ges-etmosphere mind. Receiving reverse sputtering wes performed. At that time, gss pressure wes set to 0.8Pa end sputtering time smount wss sst es for 2 minutes. By this reverse sputtering, it is the leyer insulation layer 11. It is the processing side TS upwerds. It formed.
[0042] Process (5): It is the leyer insulstion lsyer 11 by subsequently carrying out sputtering of the chromium using the ssme vecuum sputtering system. Processing side TS It is the chromium thin leyer L1 with a thickness [as e metal thin layer] of 0.1 micrometers upwsrds. It formed. Furthsrmore, it is the chromium thin leyer L1 by carrying out sputtsring of the copper using the seme vecuum sputtering system. It is the 0.2-micrometer copper thin layer L2 upwerds. It formed. Conesquently, as shown in drawing 1 (c), the substrate leyer UL with a thicknese of 0.3 micrometers it is thin from chromium and two sorts of copper metals was obtained.
[0043] In sddition, in this exemple, by sputtering of chromium, gas pressure was set to 0.8Pa and sputtering time emount wss made into 10 minutes. Moreover, in copper sputtering, gas preasure wes set to 0.8Ps snd sputtering time smount was made into 20 minutes.
[0044] The photopolymer for plsting-resist formation (Tokyo sdaptation meke, OMR- 83/60cps) wes applied on the substrate lsyer UL using process (6):, next e spin coster. In addition, it set up so thet the thickness of the plsting resist 3 finally obtained might be set to 1 micrometer. And prebeking, exposure snd development, snd postbake were performed.
[0045] Consequently, as shown in drawing 1 (d), it is a conductor pattern (last shipmsnt=30micrometer / 50 micrometers) C2. The pleting resist 3 of the shape of a channel for forming was formed on the substrste lsyer UL.
[0046] By carrying out electrolytic copper pleting using process (7):, next the following electrolytic copper plating bath, as shown in drawing 1 (e), it is the electrolytic copper plating layer L3 with a thickness of 10 micrometers on the substrate layer UL. It formed.
[0047] H2 SO4 and 5H2 O:210 g/l H2 SO4 : 60 g/l, chlorine ion:25 mg/l Additive: Smell quantity Bath temperature: 28 degrees C and cethodio current consistenoy:2.5 A/dm2 Processing time: 10 minutes
The plsting resist 3 which became unnecesary was exfoliated from the substrate layer UL by etching with procese (8):, next the exfoliation liquid (Tokyo adaptation meke, OMR exfolistion liquid) of dedication of the phosphor bronze substrate 1. Furthermore, copper thin layer L2 first loceted under pleting reeist 3 by using a nitric-acid water solution as etchsnt 10% It etched. Then, chromium thin layer L1 similsrly locsted under pleting rssist 3 by using a hydrochloric-ecid weter solution as etchant 20% It etched. consequently, it is shown in drawing 1 (f) — as — chromium thin layer L1 Copper thin layer L2 from — the becoming substrate layer UL end ths electrolytic copper plsting layer L3 Conductor pattern C2 constituted It obteined.
[0048] Process (9): By carrying out by rspeeting e process (8) from ssid process (2), thsy ere the conductor pattern C3 after ths 3rd layer - C6. Layer insulation layer 12 -15 efter the 2nd lsyer Sequential formstion was carried out. And the multilsyer-interconnsction plste 6 which hss

e build up layer as finally shown in drawing 2 was obtained.
[0049] The multilayer-interconnaction plate 6 obtained according to a serias of above-mentioned processes is used, and they are the ** conductor pattern C2 - C6. The dimensional accursacy of the width of fece of Rhine L, and ** layer insulation layer I1 -I5 The dimensional accursacy and the ** conductor pattarn C2 of thickness - C6 Pull reinforcement was investigated. Those results are shown in Tabla 1.
[0050] A conductor pattarn C2 - C6 When surveyed, it turned out that the width of face of Rhine L takes the value extramely approximated to 30 micrometers which is the set point. It turned out that the velue which similarly was extremaly approximatad to 20 micrometers which is the set point also about the thickness of layer insuletion lsyar I1 -I5 is takan. Moraover, when pull reinforcement wss meesured, the auitable velue exceeding 2.0 kgf/mm2 was acquired.
[Examples 2 and 3]
A process (1) - a process (4): It was besed on the process (1) of en example 1 - the proceas (4).

[0051] Process (5): By cerrying out sputtering of the titanium using the vecuum sputtering system mentioned above, it is the leyar insuletion layar I1. Processing eide TS It is the titanium thin layer L1 with a thicknass [as a metel thin leyer] of 0.1 micromaters upwards. It formed. Furthermora, it is the titanium thin layer L1 by carrying out sputtaring of the copper using the ssme vscuum sputtering system. It is the 0.2-micrometar copper thin layer L2 upwards. It formed. Consequently, es shown in drswing 1 (c), the substrate layer UL with e thickness of 0.3 micrometers it is thin from titanium end two sorts of copper metals wes obtained.
[0052] A process (6) - a process (9): Based on tha process (6) of en exemple 1 - the process (9), tha multileyer-interconnection plate 6 as finally shown in drswing 2 wes obtained after that. The result which the **** investigated using this multilayar-interconnection plete 6 is shown in Tebla 1. Consequently, a conductor pattern C2 - C6 Tha Rhine width of face is also layar insulation layar I1 -I5. It turned out that the velue which approximated thickness as wall es an example 1 to the set point extremely is taken. Moreovar, when pull reinforcement was measured, the suitable value exceeding 2.0 kgf/mm2 was acquired.
[0053] And as shown in Table 1, it is the metal thin layer L1. The suitabla result was obtained about the example 3 which replaced the formetion ingrediant with nickal from titanium es well as examples 1 and 2. Moreover, it is the coppar thin layer L2 only by ona sort of atchant called fluoric acid:nitric-acid =1:3 water solution the cesa of en example 3. Nickel thin layer L1 Thare was an advantage that it could etch into coincidence.
[Examplas 4-6]
Process (1): In tha example 4, tha elumina substrate (sluminum2 O3 =92%) 4 was chosen es a substrate. And it is the conductor pattern C1 of the 1st layer by carrying out sputtering of titanium, molybdenum, and the nickel on the elumine substrate 4. It formed.
[0054] Process (2): By applying the resin used in the exemple 1 using e spin coeter, it is the conductor pattern C1 of the 1st layer. It is the layar insulstion layer I1 upwards. It formed. In addition, layer insulation layer I1 finally obtained in this example 4 The thickness of the resin to apply was set as 17 micrometers so that thickness might be set to 10 micrometers.
[0055] A process (3) - a process (5): It was besed on the process (3) of an exmple 1 - the procass (5).
The photopolymer for pleting-resist formetion used in the example 1 on the substrate leyar UL using process (6):, naxt a spin coster was spplied, end prebaking, exposure end development, and postbake were parformed. Consequently, es shown in drewing 1 (d), it is a conductor pattern (last shipment=15micrometer / 20 micrometers) C2. The plating resist 3 of the shspe of a channel for forming wes formed on the substrate leyer UL.
[0056] By carrying out electrolytic copper plating using process (7):, naxt tha alactrolytic coppar plating bath used in the example 1, as shown in drawing 1 (a), it is the electrolytic coppar plating leyar L3 with a thickness of 6 micrometers on the substrate leyer UL. It formed.
[0057] A procass (8) - a process (9): Based on the process (8) of en example 1 - the process (9), the multilayer-interconnection plate 6 as finelly shown in drawing 2 was obtained aftar that. Tha rasult which the **** investigated using this multilayer-interconnection plete 6 is shown in Table 1. Consequently, e conductor pattarn C2 - C6 The Rhine width of fece is also layer insulation layar I1 -I5. It turned out that the value which approximated thickness as well as an example 1 to the set point extremely is taken. Moreover, when pull reinforcement was measured, the suitable value exceeding 2.0 kgf/mm2 was acquired.
[0058] And as shown in Table 1, it is the matal thin layer L1. The suitable result was obtained about the example 5 which replaced the formetion ingredient with titanium from chromium, and the example 6 replsced with nickel from chromium ea well as an exemple 4. Moreover, it is the copper thin layer L2 only by one sort of etchant called fluoric acid:nitric-acid =1:3 water solution the cese of an exemple 6. Nickel thin layer L1 There was an edvantage thet it could etch into coincidance.
[Examples 7-9]
Process (1): In the exemple 7, tha elumimium nitride substrate (AlN:Y2O3 =96:4) 1 wes choaen ea e substrete. And it is the conductor pettern C1 of the 1st leyer by carrying out sputtering of titanium, molybdanum, end tha nickel on the elumimium nitride substrata 1. It formad.
[0059] Process (2): By spplying the resin used in the exemple 1 using a spin coeter, it is the conductor pattern C1 of the 1st leyer. It is tha layer insuletion lsyar I1 upwards. It formed. In eddition, layer insulation layer I1 finally obtained in this example 7 The thicknees of the resin to epply wes set ea 10 micrometera eo that thickness might be set to 5 micrometers.
[0060] A process (3) - a process (5): It wes besed on the process (3) of an exemple 1 - the process (5).
The photopolymer for plating-resist formation used in the example 1 on the substrete leyer UL using process (6):, next e apin coeter was epplied, end prebeking, exposure and development, end postbeke were performad. Consequently, aa shown in drawing 1 (d), it is a conductor pattern (last shipment=4micrometer / 6 micrometers) C2. The plating reaist 3 of the shape of e channel for forming wes formed on the substrete leyer UL.
[0061] By carrying out electrolytic copper plating using process (7):, next the electrolytic copper pleting bath used in the exemple 1, aa shown in drawing 1 (e), it is the electrolytic copper plating layar L3 with a thicknesa of 1.5 micrometers on the subatrete leyer UL. It formed.
[0062] A procesa (8) - a process (9): Based on the process (8) of an example 1 - the process (9), the multilayer-interconnection plate 6 as finelly shown in drawing 2 wes obtained efter thet. The result which the **** investigeted ueing this multilayer-interconnection plete 6 is shown in Table 1.
[0063] Consequantly, in spite of very FAIN as compared with examples 1 end 2, they are e conductor pattern C2 - C6. The Rhine width of fece is also layer insulation layer I1 -I5. It turned out that the value which also epproximated thickness to the aet point extremely is taken. Subsequently, when pull reinforcement wea meaaured, the suitable value exceeding 2.0 kgf/mm2 was acquired.
[0064] And as shown in Table 1, it is the metal thin layer L1. The very suitable reault was obtained about the exmple 8 which replaced the formation ingredient with titanium from chromium, and the exmple 9 replaced with nickel from chromium es well as an exsmple 7. Moreover, it is the copper thin layer L2 only by one sort of etchant called fluoric acid:nitric-acid =1:3 weter aolution the cese of an exemple 9. Nickel thin layer L1 There was an adventage thet it could etch into coincidence.
[Example 10]
A procesa (1) - a process (4): It was baaed on the process (1) of en example 1 - the proceas (4).

[0065] Procesa (5): By cerrying out aputtering of the nickel using e vecuum sputtering system, it ia the layer insulation leyer I1. Procassing eide TS The nickel thin leyer L1 (= the substrate layer UL which consists only of one aort of metals) with a thickness of 0.1 micrometera wes formed upwards. In eddition, about the gas pressure and time amount at the time of sputtering, it appliad to the conditions of en exemple 1 correspondingly.
[0066] A process (6) - a process (7): It was based on the process (6) of an example 1 - the procesa (7).
Procesa (8): Plating rasist 3 waa first exfoliated from the substrate layer UL by etching with the

exfolistion liquid of dedication of the phosphor bronzs substrate 1. Next, the nickel thin layer L1 located under plating resist 3 20%, using a hydrochloric-acid water solution as etchant was etched. Consequently, nickel thin layer L1 And electrolytic copper plating layer L3 Conductor pattern C2 constituted It obtained.

[0067] Process (9): By carrying out by repeating a process (2) – e process (8), they are the conductor pattern C3 after the 3rd layer – C6. Layer insulation layer I2 –I5 after the 2nd layer Sequential formation was carried out. And the multilayer-interconnection plate 7 as finally shown in drawing 3 was obtained.

[0068] The result which the **** investigated using this multilayer-interconnection plate 7 is shown in Table 1. Consequently, a conductor pattern C2 – C6 The Rhine width of face is also layer insulation layer I1 –I5. It turned out that the value which approximated extremely thickness as well as the multilayer-interconnection plate 6 of example 1 grade to the set point is taken. Moreover, when pull reinforcement was measured, the suitable value exceeding 2.0 kgf/mm2 was acquired.

[0069] That is, although only one sort of metals constitute the substrate layer UL from this example 10 thinly, it will be said that the engine performance comparable as examples 1–9 is obtained. And when such a configuration is adopted, the time amount of sputtering etc. decreases and it becomes in process, in cost, and advantageous.

[Example 11]

A process (1) – e process (5): Based on the process (1) of an example 2 – e process (5), as shown in drawing 4 (a) – drawing 4 (c), it is the layer insulation layer I1. The substrate layer UL was formed upwards.

[0070] The photopolymer for resist formation (the Hoechst A.G. make, trade name:AZ–4200) was applied on the substrate layer UL using process (6):, next a spin coater. In addition, in this example, it sat up so that the thickness of the resist 5 finally obtained might be set to 3 micrometers.

[0071] And ea prebaking, exposure and development, and postbake are performed and it is shown in drawing 4 (d), it is a conductor pattern (last shipment=15micrometer / 20 micrometers) C2. The resist 5 of the shape of a channel for forming was formed on the substrate layer UL.

[0072] Copper thin layer L2 located under said resist 5 process (7):, next by using a nitric-acid water solution ea etchant 10% It atched. Then, chromium thin layer L1 similarly located under the resist 5 by using a hydrochloric-acid water solution ea etchant 20% It etched. Consequently, as shown in drawing 4 (e), the substrate layer UL was made into the shape of a predetermined pattern.

[0073] Non-electrolytic copper plating was carried out using process (8):, next the following non-electrolytic copper plating bath. It is the non-electrolytic copper plating layer L3 with a thickness of 6 micrometers on the substrate layer UL etched in the shape of a pattern by this non-electrolytic copper plating as shown in drawing 4 (f). It formed.

[0074] CuSO4 and 5H2 O:0.05 mol/l, HCHO: 0.12 mol/l and NaOH:0.15 mol/l EDTA and 4Na:0.10 mol/l, KNi3 (CN) : 10 mg/l Alpha-alpha'-DIPIRIJIRU: Small quantity, pH=12.5 Bath temperature : [60 degrees C,] processing-time: – 2 hour ., consequently chromium thin layer L1 Copper thin layer L2 from – the becoming substrate layer UL and the non-electrolytic copper plating layer L3 Conductor pattern C2 constituted It obtained.

[0075] Process (9): By carrying out by repeating said process (2) – a process (8), they are the conductor pattern C3 after the 3rd layer – C6. Layer insulation layer I2 –I5 after the 2nd layer Sequential formation was carried out. And the multilayer-interconnection plate 6 which has a build up layer as finally shown in drawing 2 was obtained.

[0076] The result which the **** investigated using this multilayer-interconnection plate 6 is shown in Table 1. Consequently, a conductor pattern C2 – C6 The Rhine width of face is also layer insulation layer I1 –I5. It turned out that the value which approximated extremely thickness as well as the multilayer-interconnection plate 6 of example 1 grade to the set point is taken. Moreover, when pull reinforcement was measured, the suitable value exceeding 2.0 kgf/mm2 was acquired.

[The example of a comparison]

process (1): – the melanism after choosing copper clad laminate (FR–4) as a substrate and forming the inner layer conductor pattern of the 1st layer according to a well-known approach conventionally – it processed.

[0077] Process (2): The photosensitive epoxy resin which consists of the following presentation as resin for layer insulation strstification was prepared, and this resin was applied on the substrate using the roll coater.

Cresol novolak acrylate resin: 53 % of the weight, bisphenol A mold resin:17 % of the weight, epoxy resin filler:19 % of the weight Sensitizer: 5 % of the weight, curing agent:2 % of the weight Photopolymerization agent: 3 % of the weight Interface regulator: The thickness of the resin to apply was set as 90 micrometers so that the thickness of the layer insulation layer which is 1 % of the weight , and which is finally obtained might be set to 55 micrometers.

Process (3): After prebeking said resin, the layer [1st] layer insulation layer was formed by [for exposure, development and 150 degrees C, and 180 minutes] carrying out cure processing.

[0078] Process (4): After roughening the front face of a layer insulation layer by processing chrome oxide (CrO3) for about 60 minutes, the Pd–Sn catalyst nucleus was given to the roughening side. Subsequently, the photosensitive epoxy resin was applied to the thickness of 30 micrometers by the roll coater. And plating resist of the shape of a channel for forming a conductor pattern (last shipment=75micrometer / 75 micrometers) was obtained by drying this resin, and exposing and developing negatives.

[0079] Process (5) :P After activating a d–Sn catalyst nucleus, non-electrolytic copper plating was carried out using the non-electrolytic copper plating bath for thickness attachment of the following presentation. With this non-electrolytic copper plating, the non-electrolytic copper plating layer with a thickness of 30 micrometers was formed in the plating-resist agenesis part.

[0080] CuSO4 and 5H2 O:0.05 mol/l HCHO:0.12 mol/l and NaOH:0.15 mol/l EDTA and 4Na:0.10 mol/l, KNi3 (CN) : 10 mg/l Alpha-alpha'-DIPIRIJIRU: Small quantity, pH=12.5 Bath temperature: 60 degrees C Processing time: 6 hours

Process (6): By carrying out by repeating said process (2) – e process (5), sequential formation of the conductor pattern after the 3rd layer and the layer insulation layer after the 2nd layer was carried out. And the additive multilayer-interconnection plate which finally has a build up layer was obtained.

[0081] The result which the **** investigated using the multilayer-interconnection plate of the example of a comparison is shown in Table 1. Consequently, the result that the dimension error of the Rhine width of face of a conductor pattern became large compared with the time of examples 1–11 was obtained. Moreover, the result with the same said of the dimension error of the thickness of a layer insulation layer was obtained. That is, in the case of the multilayer-interconnection plate of the example of a comparison, it was expected with the irregularity of the front face resulting from aggravation and roughening of the smooth nature of a layer insulation layer etc. that aggravation of the formation precision of a conductor pattern, the electrical property of a patchboard, etc. was brought about. Furthermore, when pull reinforcement was measured, it stopped at the low value of 1.0 kgf/mm2 which are a value below abbreviation one half of examples 1–11.

[0082] Moreover, when the manufacture approach of the example of a comparison was compared with the manufacture approach of examples 1–11, it was checked that production time becomes [the way of the former which needs a roughening process and a thickness attachment radio solution copper–plating process] long generally.

[0083]

[Table 1]

	基板	※1	導体パターン（μm）				絶縁層（μm）
			L1	L2	L3 ※2	L/S	
実施例1	りん青銅	①	Cr 0.1	Cu 0.2	電Cu 10	30／50	20
実施例2	りん青銅	①	Ti 0.1	Cu 0.2	電Cu 10	30／50	20
実施例3	りん青銅	①	Ni 0.1	Cu 0.2	電Cu 10	30／50	20
実施例4	Al_2O_3	①	Cr 0.1	Cu 0.2	電Cu 6	15／20	10
実施例5	Al_2O_3	①	Ti 0.1	Cu 0.2	電Cu 6	15／20	10
実施例6	Al_2O_3	①	Ni 0.1	Cu 0.2	電Cu 6	15／20	10
実施例7	AlN	①	Cr 0.1	Cu 0.2	電Cu 1.5	4／8	5
実施例8	AlN	①	Ti 0.1	Cu 0.2	電Cu 1.5	4／8	5
実施例9	AlN	①	Ni 0.1	Cu 0.2	電Cu 1.5	4／8	5
実施例10	りん青銅	①	Ni 0.1	－	電Cu 10	30／50	20
実施例11	Al_2O_3	②	Cr 0.1	Cu 0.2	無電Cu 6	15／20	10
比較例	FR－4	－	－	－	無電Cu30	75／75	55

注：※1…表中①は請求項3に記載の製造方法を示し、②は請求項4に記載の製造方法を示している。

※2…「電Cu」は電解銅めっきを意味し、「無電Cu」は無電解銅めっきを意味している。

[0084]
[Table 2]

	導体パターンのしの幅 設定値	導体パターンのしの幅 実測値	層間絶縁層の膜厚 設定値	層間絶縁層の膜厚 実測値	プル強度 (kgf/mm²)
実施例1	30	30.5±1.0 μm	20	20.0±2.5 μm	＞2．0
実施例2	30	29.6±1.5	20	20.2±3.1	＞2．0
実施例3	30	30.7±1.4	20	20.3±2.7	＞2．0
実施例4	15	14.5±1.5	10	10.0±3.0	＞2．0
実施例5	15	15.4±1.2	10	9.8±2.5	＞2．0
実施例6	15	15.3±1.3	10	10.4±2.6	＞2．0
実施例7	4	4.3±1.1	5	5.2±1.9	＞2．0
実施例8	4	3.7±0.8	5	5.1±2.0	＞2．0
実施例9	4	4.1±0.9	5	4.9±1.7	＞2．0
実施例10	30	30.2±1.5	20	19.8±2.8	＞2．0
実施例11	15	15.2±1.3	10	10.2±2.7	＞2．0
比較例	75	75.0±5.0	55	55.0±10.0	1．0

[0085] In addition, of course, modification within the limits which do not deviate from the meaning of invention, such as not being limited only to each above-mentioned example, for example, increasing or decreasing the number of layers of a build up layer, is possible for this invention.

[0086]

[Effect of the Invention] As explained in full detail above, with the multilayer-interconnection plate of this invention, the outstanding effectiveness that the conductor pattern which cannot exfoliate easily can be obtained is done so, without roughening the layer insulation layer by chemicals, since it is characterized by performing metaled sputtering which may improve the adhesion of a conductor pattern.

[0087] Moreover, by the manufacture approach of the multilayer-interconnection plate of this invention, the approach of applying the resin for forming a layer insulation layer by the spin coater is adopted. For this reason, according to this manufacture approach, the thickness control of a layer insulation layer becomes easy, and the outstanding effectiveness that it can have, and the smooth nature of a layer insulation layer and homogeneity can be raised, and adhesion, formation precision, etc. of a conductor pattern can be raised certainly is done so.

[0088] And similarly in order [according to this manufacture approach] to perform surface treatment of the layer insulation layer by reverse sputtering, roughening by chemicals becomes unnecessary. Therefore, a production process can be simplified and the outstanding effectiveness that a manufacturing cost can moreover be reduced is done so.

[Translation done.]